designing a layout of a second gate electrode of a second MOS transistor on said active area, one end of said second gate electrode extending to an outside of said active area across the second edge in a vertical direction to the first direction,

Cont. B7

wherein a length y from the second edge to the one end of said second gate electrode is longer than a length x from the first edge to the one end of said first gate electrode wherein $y = x + \alpha$ where $0 < \alpha \leq x$.

REMARKS

This amendment responds to the Office Action dated August 9, 2000 in which the Examiner rejected claims 1 and 12 under 35 U.S.C. § 102(e).

Claim 1 claims a semiconductor device comprising an active area and an insulating film. The active area is provided with at least one MOS transistor. The insulating film defines the active area. The active area is set in a shape having a concave part in a shape along a plan view. The active area is provided with an ordinary region and a depressed region having an edge portion which is depressed beyond the ordinary region due to the presence of the concave part. The at least one MOS transistor includes first and second MOS transistors. The first MOS transistor is formed in the depressed region. The second MOS transistor is formed on the ordinary region. A length of a margin part of a first gate electrode constructing the first MOS transistor in the depressed region is set to be larger than that of a margin part of a second gate electrode constructing the second MOS transistor in the ordinary region. A length of the margin part of the second gate electrode is X. The length of the margin part of the first gate electrode is $X + \alpha$ where $0 < \alpha \leq X$.

Through the structure of the present invention a) having first and second MOS transistors, each having a margin part and b) the length of the margin part of the first gate electrode is larger than that of the margin part of the second gate electrode, as claimed in claim 1, the present invention provides a semiconductor device in which an end portion of the first gate electrode completely reaches an upper portion of the insulating film so that the first gate electrode is prevented from partial reduction of the gate length and therefore prevents occurrence of current leakage between source/drain regions which are formed on the exterior of both side surfaces of the first gate electrode. The prior art does not show, teach or suggest first and second MOS transistors each having a margin part where the length of the margin part of the first gate electrode of the first transistor is larger than the margin part of the second gate electrode of the second transistor as claimed in claim 1.

Claim 12 claims a method of fabricating a semiconductor device on the basis of a layout design, the layout design is achieved by a process comprising the steps of; first, designing a layout of an active area on a plane. The active area is defined from an insulating film by a boundary including a first edge extending along a first direction and a second edge extending along the first direction and a third edge connected between one ends of the first and second edges extending along a second direction different from the first direction. The first to third edges form a step shape so that the second edge is depressed toward an inside of said active area beyond the first edge. Next, a layout of a first gate electrode of a first MOS transistor on the active area is designed. One end of the first gate electrode extends to an outside of the active area across the first edge in a vertical direction to the first direction. Finally, a layout of a second gate electrode of a second

MOS transistor on the active area is designed. One end of the second gate electrode extends to an outside of the active area across the second edge in a vertical direction to the first direction. A length y from the second edge to the one end of the second gate electrode is longer than a length x from the first edge to the one end of the first gate electrode where $y = x + \alpha$ where $0 < \alpha \leq x$.

Through the method of the present invention having a length y from the second edge to the one end of the second gate electrode being longer than a length x from the first edge to the one end of the first gate electrode, where $y = x + \alpha$ and where $0 < \alpha \leq x$, as claimed in claim 12, the present invention provides a method of forming a semiconductor device in which an end portion of the first gate electrode completely reaches an upper portion of the insulating film so that the first gate electrode is prevented from partial reduction of the gate length. The prior art does not show, teach or suggest the method as claimed in amended claim 12.

Claim 1 was rejected under 35 U.S.C. §102(e) as being anticipated by *Shou et al.* (U.S. Patent No. 5,811,859).

Shou et al. appears to disclose a LSI pattern of inverted amplifier INV consisting of three stages MOS inverters I1, I2 and I3. For the inverters I1 and I2, there are shaped a common P-type semiconductor layer PL1 and a common N-type semiconductor layer NL1. Drain voltage Vdd and source voltage Vss are connected to PL1 and NL1 through contacts C1 and C2. The semiconductor layers PL1 and NL1 are provided with contacts C3 and C4 for input from the first stage, respectively, and are provided with contacts C5 and C6 for an output from the second stage, respectively. A strangulation portion S1 is provided

between the contacts C1 and C5 in the semiconductor layer PL1, and a strangulation portion S3 is provided between the contacts C2 and C6 in the semiconductor layer NL1. The strangulation means S1 limit an electric current in the output of the inverter I2, and it simultaneously decreases parasitic capacity of a transistor included in the inverter I2 by decreasing electric currency.

Thus, *Shou et al.* merely discloses a first gate G passing through a strangulation portion and a second gate G ending at the end of the P-type semiconductor layer PL1. Thus, nothing in *Shou et al.* shows, teaches or suggests that the gate electrode of the second transistor formed in the ordinary region has a margin part having a length x as claimed in claim 1. Rather, *Shou et al.* teaches away from the present invention since Figure 3 of *Shou et al.* clearly discloses that the gate electrode ends at the end of the common P-type semiconductor layer PL1 (i.e., the gate does not protrude from PL1). Thus, nothing in *Shou et al.* discloses a margin part having a length x for the transistor in the ordinary region as claimed in claim 1.

Additionally, since nothing in *Shou et al.* shows, teaches or suggests a margin part of a second gate electrode of the transistor in the ordinary region, nothing in *Shou et al.* shows, teaches or suggests that a margin part of a first gate electrode of the transistor formed on the depressed region is larger than the margin part of the gate electrode of the transistor formed on the ordinary region as claimed in claim 1. Rather, *Shou et al.* teaches away from the present invention and merely discloses a gate electrode of a transistor formed on a strangulation region has a margin part while the gate electrode of the transistor

formed on the common P-type semiconductor region has no margin part (i.e., *Shou et al.* does not teach a margin part for each transistor gate).

Since nothing in *Shou et al.* shows, teaches or suggests a) a transistor formed on an ordinary region having a gate electrode having a margin part or b) a length of a margin part of a gate electrode of a transistor formed on a depressed region is larger than a margin part of a gate electrode of a transistor formed on an ordinary region, as claimed in claim 1, it is respectfully requested that the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §102(e).

Claim 12 was rejected under 35 U.S.C. § 102(e) as being anticipated by *Jassowski et al.* (U.S. Patent No. 5,668,389).

Jassowski et al. appears to disclose in Fig. 2 a portion of an exemplary cell 9. The cell 9 is a typical cell of semiconductor devices which may be positioned on a semiconductor substrate as a portion of a group of cells which provide some larger circuit function. The individual cells 9 in each row are each aligned to utilize these power buses so that the power buses 12 and 14 lie within but near to the boundaries of all of the typical cells 9. Once the cells 9 and all other portions of the larger circuit have been laid out, connections are provided between the individual cells 9 and other circuit elements which are carried on the particular substrate.

Thus, *Jassowski et al.* merely discloses on the attached Fig. 2 of *Jassowski et al.* two margin parts labeled 2 and 3. However, the margin part 3 is formed in the ordinary region and has a length greater than the margin part 2 formed in the depressed region. Thus nothing in the *Jassowski et al.* reference shows, teaches or suggests that the length

from the second edge to the one end of the second gate electrode is longer than the length from the first edge to the one end of the first gate electrode as claimed in claim 12. Rather, *Jassowski et al.* appears to be the opposite of the present invention and discloses that the length from the first edge is longer than the length from the second edge.

Furthermore, although *Jassowski et al.* discloses a margin 1, the length of this margin does not fall into the equation as claimed in amended claim 12 and in particular that the length from the second edge is greater than the length from the first edge by $\propto$ where $0 < \propto \leq x$ as claimed in claim 12.

Since nothing in *Jassowski et al.* shows, teaches or suggests a length y from the second edge to the one end of the second gate electrode is longer than the length x from the first edge to the one end of the first gate electrode where $y = x + \propto$ and $0 < \propto \leq x$ as claimed in claim 12, it is respectfully requested that the Examiner withdraws the rejection to claim 12 under 35 U.S.C. § 102(e).

Since claim 2 depends from a generic claim it is respectfully requested that the Examiner allow claim 2.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for allowance, it is respectfully requested that the Examiner enters this amendment for purposes of appeal.

If for any reason the Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the

Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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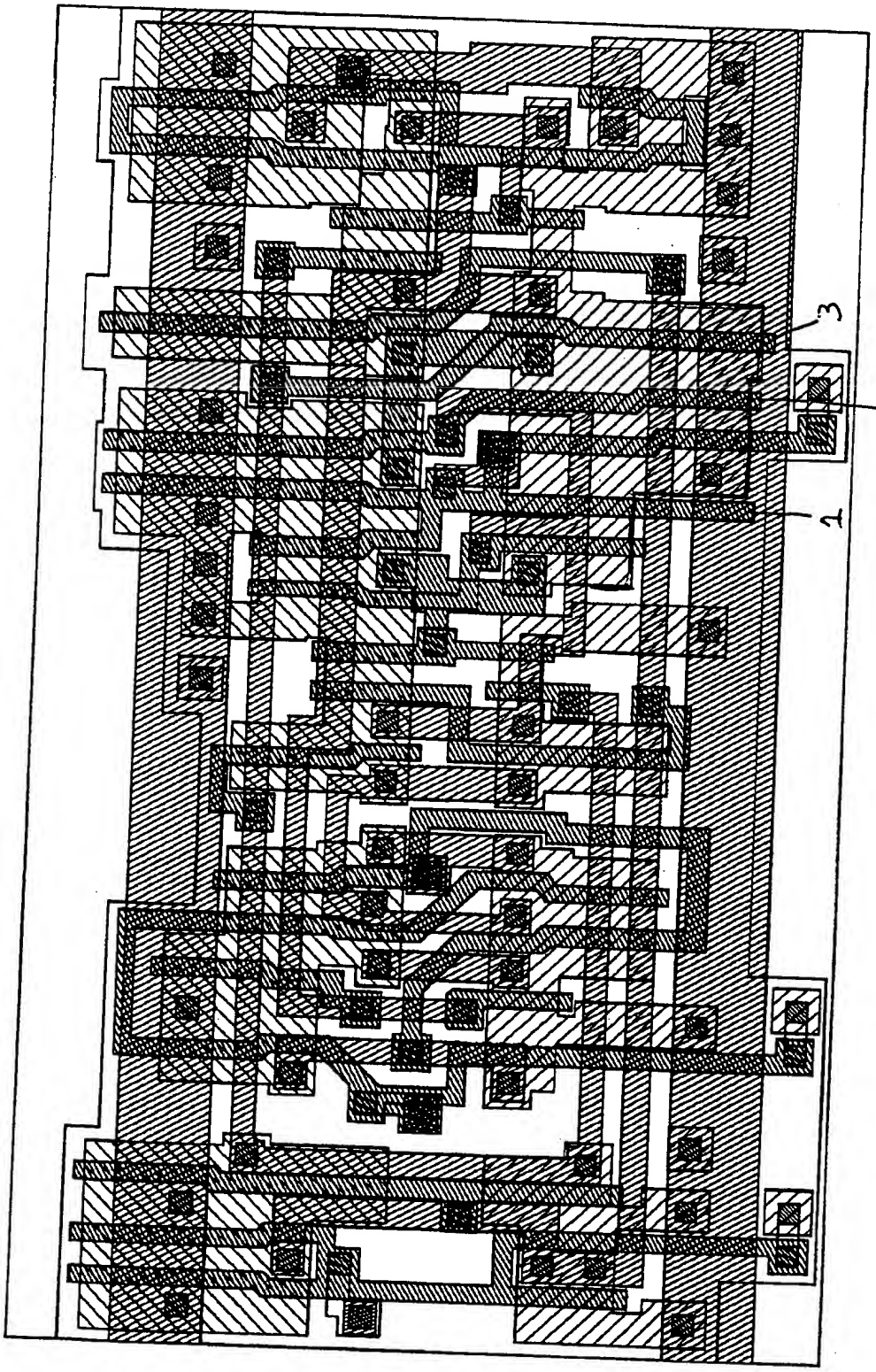

FIG_2